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ORIGINAL RESEARCH

A non-isolated single-switch ultra-high step-up DC–DC converter with coupled inductor and low-voltage stress on switch

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Abstract

This paper presents a non-isolated single-switch ultra-high step-up (UHSU) DC–DC converter with a three-winding coupled inductor (CI) which is utilized to achieve ultra-high voltage gain with a small amount of duty cycle leading to low conduction losses of the power switch and higher efficiency. The voltage gain of the suggested UHSU converter is adjusted by two methods: the duty cycle of the power switch and the three-winding CI turn ratio, therefore enhancing the design flexibility of the suggested converter. Due to the utilization of the passive clamp circuit in the structure of the proposed converter, it is possible to select a power switch with low voltage rated and small ON-state resistance, further enhancing the converter efficiency. The operation modes are discussed in detail and to clarify the salient features of the proposed converter, a comparison with other configurations is provided. Finally, to accredit the performance of the proposed converter, a 150-W laboratory archetype with an input and output voltage of 20 and 300 V, respectively, at 50 kHz switching frequency is fabricated.

1 | INTRODUCTION

Incontrovertibly, the improvement of high step-up DC–DC converters with different topologies is important in many applications. High step-up DC–DC circuits are not only popular in clean energies like photovoltaic or wind turbines. They are also popular in industry, physical, military, medical, transportation, aerospace, and many other applications that need input voltage boosting [1–3]. Ideally, if the duty cycle of the power switches increases and reaches to close 1, the step-up structure can achieve a high-voltage gain. However, because of the non-ideality of the step-up circuit and its inherent resistance, conduction losses are higher and cause serious diode reverse-recovery problems when the duty cycle of the power switches is severely large, therefore, affecting converter efficiency [4, 5].

Different voltage boost techniques have been utilized on step-up DC–DC converters by researchers to achieve a high-voltage gain without severely large duty cycles. Figure 1 demonstrates a vast classification of the voltage-boosting techniques that the voltage boosting techniques are derived from five sections (1) multi-stage/level; (2) switched capacitor (SC) (charge pump); (3) voltage multiplier; (4) switched inductor and voltage lift (VL); (5) magnetic coupling.

Utilizing a multi-stage/level technique is the first way to enhance the voltage gain of DC–DC structures that comprise three sections (1) cascade, (2) interleave, (3) multilevel. The drawbacks of these converters contained complex control schemes, a large number of components, and the high cost of the system. In [24] and [28], interleaved structures are proposed that are suitable for Photovoltaic (PV) applications because of their input ripples. The SC is one of the popular voltage-boosting techniques based on the charge pump concept that is utilized in [6, 7] to achieve high gain in DC–DC circuits. In SC-based circuits, the main disadvantage is that high instantaneous currents flow via the capacitors. High instantaneous currents flow leading to more power losses and electromagnetic noises. The voltage multiplier technique made converters more efficient and the cost of converters that use the voltage multiplier technique is low. Voltage multiplier circuit topologies are

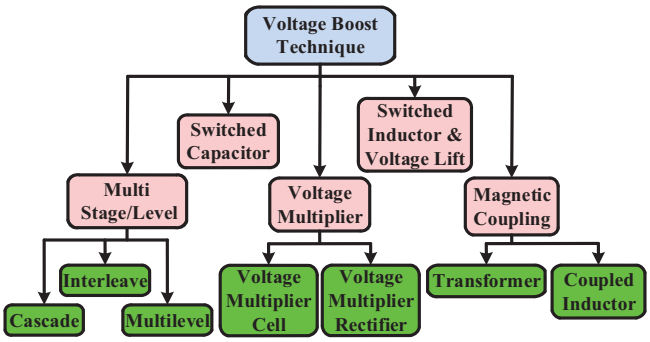

FIGURE 1 Vast categorization of voltage boost techniques utilized for DC–DC converters.

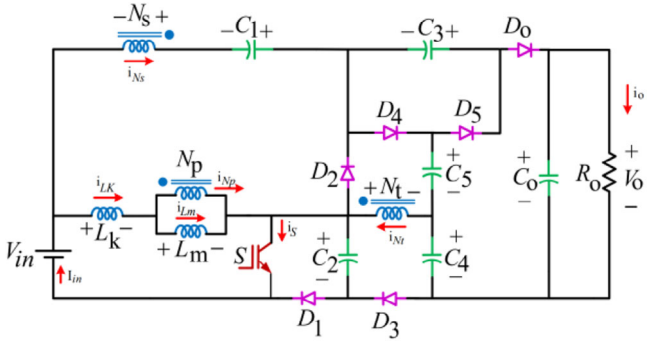

FIGURE 2 Power circuit of the proposed converter.

simple and typically manufactured by diodes and capacitors to obtain high-voltage gain [8, 9] and [27]. In [24] and [25], the voltage multiplier technique is used and high-voltage gain can be achieved but a high number of components enhance the cost and size of the converter. The main drawback of voltage multiplier circuits is high-voltage stress on components. The VL technique is one of the approbated methods that are widely utilized in DC–DC circuits to increase the input voltage and obtain high-voltage gain [10]. The VL technique is leaning on charging a capacitor to a required voltage and boosting the output voltage with the voltage level of the charged capacitor. This process repeats and using other capacitors can help to enhance the output voltage level, called re-lift, triple-lift, and quadruple-lift structures. Switched inductor technique (SL) is derived from the passive switched-inductor unit (PSL) and active switched-inductor unit (ASL). ASL cells are comprised of active switches and inductors and PSL cells consist of diodes and inductors. In [11] by combining the PSL and ASL structures high gain voltage is obtained and voltage stress across the power switches is low. The VL and SL techniques are amenable in many converters but they need more passive components, and they are not proper for high-power applications. The magnetic coupling technique is a brilliant candidate for high step-up circuits. Utilizing the CI in converters diminishes the number of components in mutuality to the discrete inductors. Converters with the coupled inductor (CI) base provide another degree of freedom because of their turn ratio. The turns ratio of the CI can increase the voltage gain of converters extremely [12–32]. The high-voltage gain of the CI-based converters can happen by varying the turns ratio between the primary, secondary, and tertiary. In [30–32], quadratic base exists that despite conventional quadratic base they do not have limitation of voltage and these converters use CI to improve the gain. Using the different types of clamp circuits like diode clamps [19], passive clamps [20, 22], and active clamps [21] reduces the voltage spikes across the power switches and also causes lower voltage stress on power switches.

This paper proposes a non-isolated single-switch high step-up DC–DC converter with coupled inductor technique that voltage stress across the power switch is low because of the passive clamp structure. The proposed converter has a three-winding CI that can achieve high-voltage gain with a varying turns ratio of the CI. Most of the Z-source (ZS) or quasi-Z-source (QZS) converters suffer from the limitation of the duty cycle because the voltage gain of these converters is inversely proportional to (1-2D), but the limitation of the duty cycle does not exist in the proposed converter and we can adjust duty cycle from 0 to 1 for achieving high-voltage gain.

The significant merits of the proposed converter are as follows:

(1) To control the converter's voltage gain we have two degrees of freedom in the proposed converter: the duty cycle of the single switch and the turns-ratio of the CIs, therefore the design of the proposed converter is flexible.
(2) By using a single power switch, a simple control process can be achieved.
(3) Unlike the ZS and QZS converters that the range of the duty cycle is between 0 and 0.5, the suggested converter achieves high-voltage gains without duty cycle limitation and we can vary the duty cycle from 0 to 1.
(4) By utilizing a passive clamp circuit, the voltage across the clamp capacitor is equal to the voltage across the power switch; thus, the voltage spikes across the single power switch are suppressed.
(5) Voltage stress of the single power switch is low; hence, a low-voltage-rating switch with a small on-resistance can be utilized to diminish conduction loss and as a result high efficiency.
(6) The suggested structure can generate high output voltage with a small duty cycle that reduces the conduction loss of the single power switch.

2 | PROPOSED CONVERTER AND OPERATION MODES

The power circuit of the proposed converter is demonstrated in Figure 2. The proposed converter comprises one power switch (S_1), six capacitors (C_1–C_5 and C_O), six diodes (D_1–D_5 and D_O), and one three-winding coupled inductor that includes N_P (number of primary side winding), N_S (number of secondary side winding), and N_t (number of tertiary side winding). Moreover, the turns ratio of the coupled inductor is $n_1 = N_S / N_P$ and $n_2 = N_t / N_P$, and the coupling coefficient is determined as $k = L_m / (L_m + L_k)$. The proposed ultra-high step-up

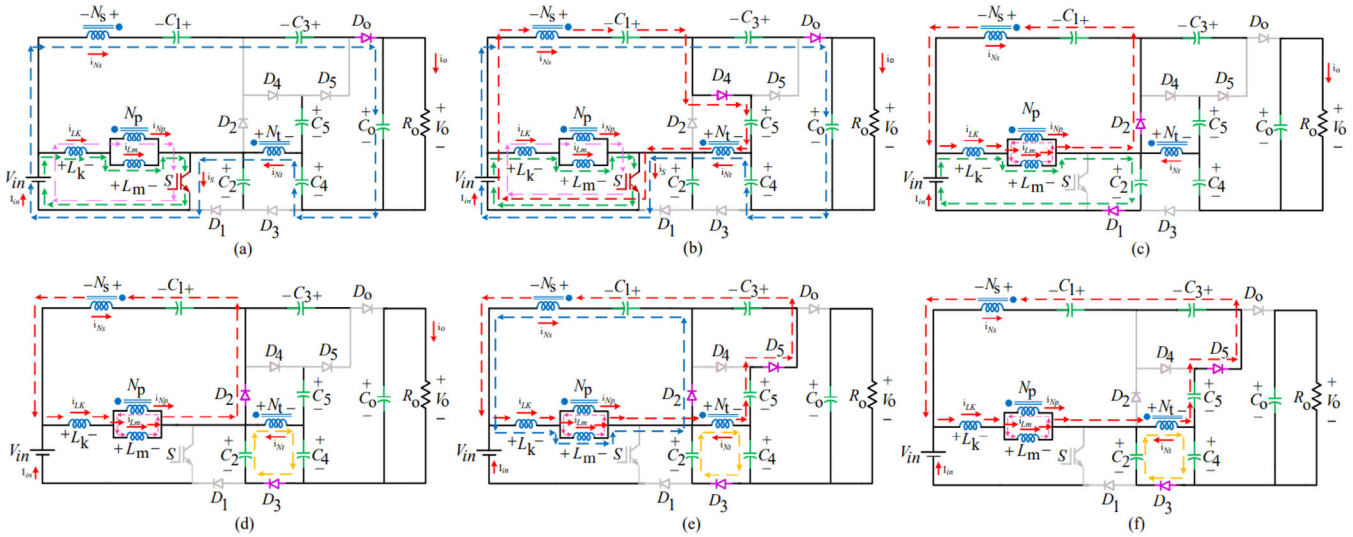

FIGURE 3 Equivalent circuits of the proposed converter in boost mode. (a) First switching subinterval, (b) second switching subinterval, (c) third switching subinterval, (d) fourth switching subinterval, (e) fifth switching subinterval, (f) sixth switching subinterval.

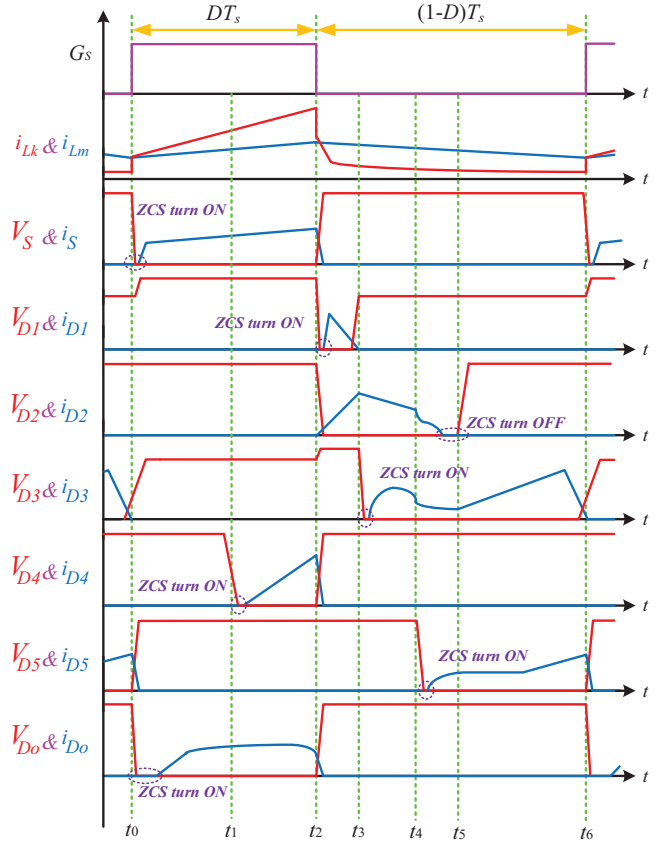

FIGURE 4 Main waveforms of the proposed converter.

(UHSU) converter in continuous conduction mode (CCM) has six subintervals which are depicted in Figure 3 and the main waveforms of the voltage and current of the components are demonstrated in Figure 4.

First switching subinterval: In this mode, power switch S is turned on and output diode D_O begins to conduct under zero current switching (ZCS) conditions, whereas the rest of the diodes are reverse-biased. The magnetizing inductor L_m is charged by the input voltage V_{in} and i_{Lm} increases linearly. The voltage input and capacitors of C_1, C_3, and C_4 have released their energy to output voltage V_O through the loop V_{in}, N_S, C_1, C_3, D_O, V_O, C_4, N_t, and S. In this time interval, according to Kirchhoff's Voltage Law (KVL), the relationships are as follows:

$$V_{Ns} = n_1 V_{Lm} \tag{1}$$

$$V_{Nt} = n_2 V_{Lm} \tag{2}$$

$$V_1 = V_{Lm} + V_{Lk} = \frac{V_{Lm}}{k} \tag{3}$$

$$V_1 = V_{in} \tag{4}$$

$$V_O = V_1 + V_{Nt} + V_{C4} + V_{C3} + V_{C1} + V_{Ns} \tag{5}$$

Second switching subinterval: In this time interval, power switch S is turned on, also diode D_O still is on and diode D_4 begins to conduct. The rest of the diodes are reverse-biased. In this mode, the magnetizing inductor L_m is charged by the input voltage V_{in} and i_{Lm} increases linearly. The output voltage V_o is charged by the voltage input and capacitors of C_1, C_3, and C_4 through the loop V_{in}, N_S, C_1, C_3, D_O, V_O, C_4, N_t, and S. The capacitor C_1 charged C_5 through the loop V_{in}, N_s, C_1, D_4, C_5, N_t, and S. According to KVL, the relationships of this mode are as

$$V_1 = V_{in} \tag{6}$$

$$-V_{C5} + V_1 + V_{Nt} + V_{C4} + V_{C1} + V_{Ns} = 0 \tag{7}$$

$$-V_{C5} - V_{C3} + V_O - V_{C4} = 0 \tag{8}$$

Third switching subinterval: In this mode, power switch S is turned off and diodes of D_1 and D_2 are forward-biased. The other diodes were turned off, and the capacitor C_2 is charged by L_m by the loop V_{in}, L_m, C_2, and D_1. The capacitor C_1 is charged through the L_m, D_2, C_1, and N_s. By applying KVL, the relationships of this mode are as

$$V_{in} - V_1 - V_{C2} = 0 \tag{9}$$

$$V_1 + V_{C1} + V_{Ns} = 0 \tag{10}$$

$$V_{in} - V_{C2} + V_{C1} + V_{Ns} = 0 \tag{11}$$

Fourth switching subinterval: In this mode, switch S is turned off and diode D_2 is still turned on along with diode D_3. In this time interval, capacitor C_1 is charged by the magnetizing inductor L_m through L_m, D_2, C_1, and N_S, and capacitor C_4 is charged by capacitor C_2 through the loop C_2, N_t, C_4, and D_3. The relationships of this mode by applying KVL are as follows:

$$V_1 + V_{C1} + V_{Ns} = 0 \tag{12}$$

$$-V_{C2} + V_{C4} + V_{Nt} = 0 \tag{13}$$

Fifth switching subinterval: In this time interval, power switch S is turned off and diodes D_2 and D_3 are still forward-biased. The diode D_5 begins to turn on and the magnetizing inductor L_m and capacitor C_5 release their energy to the capacitors C_1 and C_3 through the loop L_m, N_t, C_5, D_5, C_3, C_1, and N_s. In this mode capacitor C_2 released energy to the C_4 through the loop C_2, N_t, C_4, and D_3. The magnetizing inductor L_m discharged and released energy to the capacitor C_1 through the L_m, D_2, C_1, and N_s. By applying KVL, the equations are as

$$V_1 + V_{C1} + V_{Ns} = 0 \tag{14}$$

$$-V_{C2} + V_{C4} + V_{Nt} = 0 \tag{15}$$

$$V_{Nt} - V_{C5} + V_{C3} = 0 \tag{16}$$

$$-V_{C4} - V_{C5} + V_{C3} + V_{C1} + V_{Ns} + V_1 + V_{C2} = 0 \tag{17}$$

$$V_{Nt} - V_{C5} + V_{C3} + V_{C1} + V_{Ns} + V_1 = 0 \tag{18}$$

Sixth switching subinterval: In this mode, switch S is off and diodes D_3 and D_5 are forward-biased. The rest of the diodes are off and capacitor C_2 released energy to the capacitor C_4 through the loop C_2, N_t, C_4, and D_3. The capacitors C_1 and C_3 are charged by L_m and capacitor C_5 through the loop L_m, N_t, C_5, D_5, C_3, C_1, and N_s. The equations are as

$$-V_{C2} + V_{C4} + V_{Nt} = 0 \tag{19}$$

$$V_{Nt} - V_{C5} + V_{C3} + V_{C1} + V_{Ns} + V_1 = 0 \tag{20}$$

$$-V_{C4} - V_{C5} + V_{C3} + V_{C1} + V_{Ns} + V_1 + V_{C2} = 0 \tag{21}$$

2.1 | Voltage gain calculation

Volt's second balance law for CI can be utilized as

$$\langle V_{Lm} \rangle_{T_S} = 0 \tag{22}$$

$$\langle V_1 \rangle_{T_S} = 0 \tag{23}$$

The capacitor voltages derived from Equations (24), (25), (26), (27), and (28) are as

$$V_{C1} = \frac{DV_{in}(kn+1)}{1-D} \tag{24}$$

$$V_{C2} = \frac{V_{in}}{1-D} \tag{25}$$

$$V_{C3} = \frac{V_{in}(2kn+1)}{1-D} \tag{26}$$

$$V_{C4} = \frac{V_{in}(Dkn+1)}{1-D} \tag{27}$$

$$V_{C5} = \frac{V_{in}(2kn-Dkn+1)}{1-D} \tag{28}$$

By substituting (26), (27), and (28) into (8) the output voltage calculated by (29) is as

$$V_O = \frac{V_{in}(4kn+3)}{1-D} \tag{29}$$

Ignoring the coefficient of the coupled inductor (in fact for $k = 1$), the output voltage gain can be expressed by

$$G = \frac{V_O}{V_{in}} = \frac{(4n+3)}{1-D} \tag{30}$$

2.2 | Voltage stresses of semiconductors

The voltage stress across the power switch and diodes can be expressed by

$$V_S = \frac{V_{in}}{1-D} \tag{31}$$

$$V_{D1} = \frac{V_{in}}{1-D} \tag{32}$$

$$V_{D2} = \frac{V_{in}(kn+1)}{1-D} \tag{33}$$

$$V_{D3} = \frac{V_{in}kn}{1-D} \tag{34}$$

$$V_{D4} = \frac{V_{in}(2kn+1)}{1-D} \tag{35}$$

$$V_{D5} = \frac{V_{in}(2kn+1)}{1-D} \tag{36}$$

$$V_{Do} = \frac{V_{in}(2kn+1)}{1-D} \tag{37}$$

2.3 | Average currents of semiconductors

The average currents of the power switch and all diodes can be expressed as

$$I_S = \frac{I_o(D+4n+2)}{1-D} \tag{38}$$

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D5} = I_{Do} = I_o \tag{39}$$

2.4 | Boundary condition

For the CCM operation of the suggested converter, the minimum current of the coupled inductor must be more than zero. The minimum current of the coupled inductor and Δ_{iLm} can be calculated as

$$I_{Lm} = \frac{(4n+3)I_o}{1-D} \tag{40}$$

$$\Delta I_{Lm} = \frac{V_{in}D}{L_m f_s} \tag{41}$$

$$\begin{cases} I_{Lm,\min} = I_{Lm} - \frac{\Delta I_{Lm}}{2} \\ I_{Lm,\max} = I_{Lm} + \frac{\Delta I_{Lm}}{2} \end{cases} \tag{42}$$

$$L_m \geq \frac{D(1-D)^2 R}{2(4n+3)^2 f_s} \tag{43}$$

Normalized coupled inductor time constant can be written as

$$\tau = \frac{2L_m f_s}{R} \tag{44}$$

The boundary-normalized coupled inductor time constant can be written by utilizing (40), (41), (42), and (43).

$$\tau_B = \frac{D(1-D)^2}{(4n+3)^2} \tag{45}$$

In the CCM operation τ should be greater than τ_B. In the discontinuous conduction mode (DCM) τ_B is greater than τ and in boundary conduction mode (BCM) τ and τ_B must be equal.

$$\begin{cases} \tau > \tau_B; CCM \\ \tau < \tau_B; DCM \\ \tau = \tau_B; BCM \end{cases} \tag{46}$$

The presented converter can operate in various regions depending on Equation (46) as illustrated in Figure 5.

3 | EFFICIENCY CALCULATION

In this section, the conduction and switching losses of the suggested structure are calculated to achieve efficiency. Therefore,

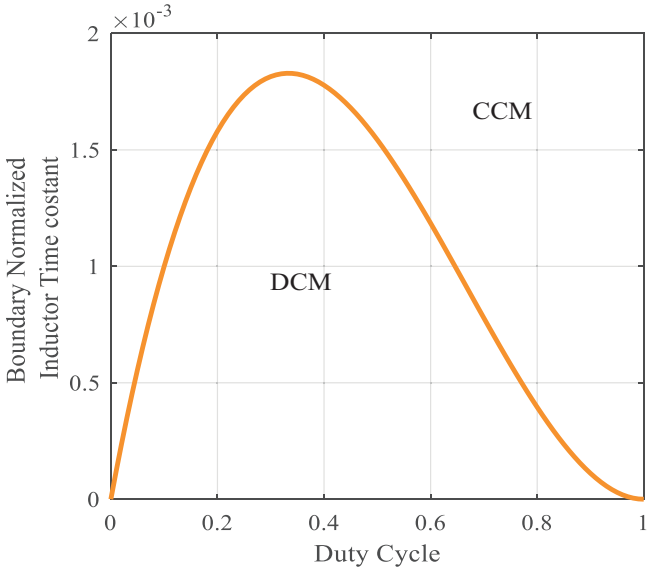

FIGURE 5 Boundary normalized inductor time constant versus duty cycle.

the internal resistors of diodes (r_D), power switch (r_S), inductor (r_{Lm}), capacitors (r_C), forward drop voltage of diodes (V_{FD}), and forward drop voltage of switch (V_F) are determined for the calculation of the power losses. Thus, the conduction and switching losses of the power switch and diodes are calculated as

$$P_{Cond,S} = \frac{Dr_s(2I_O + 4I_O n + DI_O)^2}{(D-1)^2} - \frac{DV_{Fs}(2I_O + 4I_O n + DI_O)}{D-1'} \tag{47}$$

$$P_{Cond,D_1} = 0.1 \times I_o (1-D)\left(V_{FD_1} + I_O r_{D_1}\right) \tag{48}$$

$$P_{Cond,D_2} = 0.5 \times I_o (1-D)\left(V_{FD_2} + I_O r_{D_2}\right) \tag{49}$$

$$P_{Cond,D_3} = 0.9 I_o (1-D)\left(V_{FD_3} + I_O r_{D_3}\right) \tag{50}$$

$$P_{Cond,D_4} = 0.5(Dr_{D_4} I_o^2 + DV_{FD_4} I_o) \tag{51}$$

$$P_{Cond,D_5} = \frac{2I_O (1-D)\left(V_{FD_5} + I_O r_{D_5}\right)}{3} \tag{52}$$

$$P_{Cond,D_O} = DI_o + \left(V_{FD_O} + I_o r_{D_O}\right) \tag{53}$$

$$P_{SW,S} = \frac{1}{6} \times f_s \times \frac{I_O V_{in}(D+4n+2)}{(D-1)^2}(t_{on} + t_{off}) \tag{54}$$

$$P_{SW,D_1} = \frac{1}{6} f_s I_{rr} t_b \frac{V_{in}}{1-D} \tag{55}$$

$$P_{SW,D_3} = \frac{1}{6} f_s I_{rr} t_b \frac{V_{in} n}{1-D} \tag{56}$$

$$P_{SW,D_4} = \frac{1}{6} f_s I_{rr} t_b \frac{V_{in}(2n+1)}{1-D} \quad (57)$$

$$P_{SW,D_5} = \frac{1}{6} f_s I_{rr} t_b \frac{V_{in}(2n+1)}{1-D} \quad (58)$$

$$P_{SW,D_O} = \frac{1}{6} f_s I_{rr} t_b \frac{V_{in}(2n+1)}{1-D} \quad (59)$$

The total power loss of the power switch and diodes (switching and conduction loss) is expressed as

$$P_{S,Tot} = P_{Cond,S} + P_{SW,S} \quad (60)$$

$$P_{D,Tot} = P_{Cond,D_{1,2,3,4,5,o}} + P_{SW,D_{1,3,4,5,o}} \quad (61)$$

The conduction loss of the magnetizing inductor L_m is written as the following equation:

$$P_{Cond,Lm} = r_{Lm} I_{Lm}^2 = r_{Lm} \left[-\frac{\text{Io}\,(4n+3)}{D-1} \right]^2 \quad (62)$$

The core power loss related to the CI is expressed as

$$P_C = k f_s^{\alpha} B_m^{\beta} \quad (63)$$

The power loss of the coupled inductor core (P_C) is in unit W/kg. The employed coefficients of the core are α, β, and k and they are called Steinmetz parameters which are sometimes supplied by manufacturers for distinct core materials. The values of the α coefficient can modify from 1 to 2 for ferrite materials ($1 \leq \alpha \leq 2$). Under Faraday's Law, it might be expressed as

$$V_L = N \frac{d\varphi(t)}{dt} = N A_c \frac{dB(t)}{dt} \quad (64)$$

where Ac is the core area that is introduced via manufacturers for various types of magnetic cores. N is the turn ratio of the coupled inductor. Therefore, the peak flux density of ΔB for the CI is achieved as

$$\Delta B = \frac{1}{N A_c} \int_0^{DT_s} V_L dt = \frac{V_{in} D T_s}{N_P A_c} = \frac{V_{in} D}{N_P A_c f_s} \quad (65)$$

The core loss for the CI is equal to $P\text{Core} = PCM$, where M is the mass of the coupled inductor core. Thus, considering $B\text{m} = \Delta B/2$, the core loss is defined as

$$P_{Core} = k f_s^{\alpha} \left(\frac{V_{in} D}{2 N_P A_c f_s} \right)^{\beta} M \quad (66)$$

Based on a book entitled, 'Transformer and Inductor Design Handbook' written by Colonel Wm. T. McLyman, the characteristics utilized for calculating core losses are as $k = 5.597 \times 10^{-4}$, $\alpha = 1.43$, $\beta = 2.85$, $B_m = 0.2$ T, $M = 0.15$ kg, $f_s = 50$ kHz.

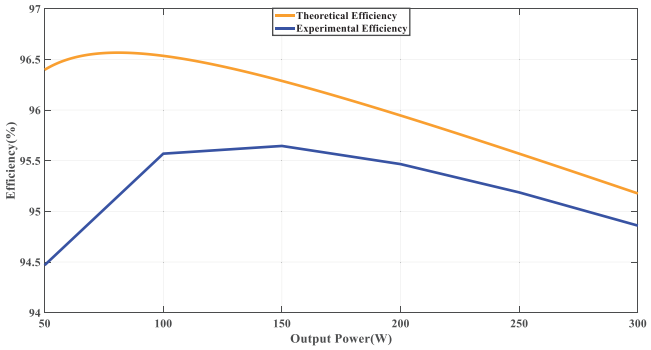

FIGURE 6 The theoretical and experimental efficiency of the proposed step-up topology versus output power.

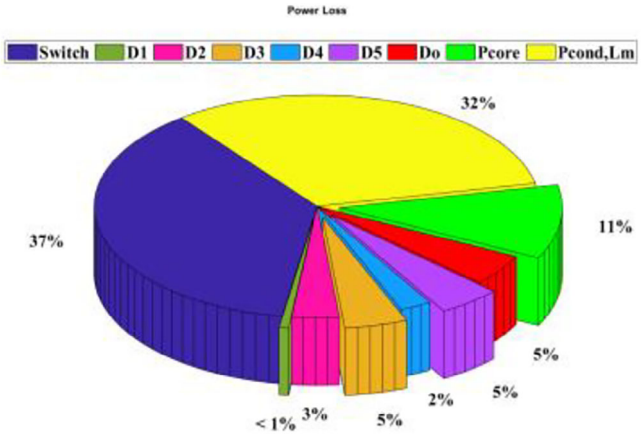

FIGURE 7 Calculated power loss percentages for the components ($P_O = 150$ W, $V_{in} = 20$ V, and $Vo = 300$ V).

Hence, the total power losses P_{Loss} for the UHSU structure are calculated as

$$P_{Loss} = P_{S,Tot} + P_{D,Tot} + P_{Cond,Lm} + P_{Core} \quad (67)$$

The efficiency of the suggested converter (η) is calculated as

$$\eta = \frac{P_{Out}}{P_{Out} + P_{Loss}} \quad (68)$$

where P_{Out} is the output power of the suggested converter which is expressed as $P_{Out} = V_O^2 / R_O$.

The theoretical and experimental efficiency of the suggested circuit versus output power is plotted in Figure 6. Therefore, referring to (47) to (68), the analytical efficiency of the suggested circuit can be obtained. Figure 7 depicts power loss percentages for each kind of the components.

4 | KEY PARAMETER DESIGN GUIDANCE

4.1 | Capacitors voltage ripple in boost mode

The characteristic design of the capacitors is based on the average of capacitor currents during all switching subintervals, the voltage of the capacitors, the duty cycle, the permitted

fluctuation range $x_C\%$, and the switching frequency that is considered 50 kHz. Therefore, the minimum values of capacitors C_1–C_O can be calculated as follows:

$$C_1 \geq \frac{2I_O \times (1-D)}{f_s \times D \times V_{in} \times (kn+1) \times x_{C1}\%} \tag{69}$$

$$C_2 \geq \frac{I_O \times (1-D)}{f_s \times V_{in} \times x_{C2}\%} \tag{70}$$

$$C_3 \geq \frac{I_O \times (1-D)}{f_s \times V_{in}(2kn+1) \times x_{C3}\%} \tag{71}$$

$$C_4 \geq \frac{I_O \times (1-D)}{f_s \times V_{in} \times (Dkn+1) \times x_{C4}\%} \tag{72}$$

$$C_5 \geq \frac{I_O \times (1-D)}{f_s \times V_{in} \times (2kn - Dkn + 1) \times x_{C5}\%} \tag{73}$$

$$C_O \geq \frac{I_O \times (1-D)}{f_s \times V_{in} \times (4kn+3) \times x_{CO}\%} \tag{74}$$

4.2 | Coupled inductor design

The characteristic design of the CI is based on the average of CI currents, the voltage across coupled inductor during all switching subintervals, the duty cycle, the permitted fluctuation range $x_L\%$, and the switching frequency. Hence, the minimum value of the magnetizing inductor is expressed as

$$L_m \geq \frac{V_{in} \times D \times (1-D)}{f_s \times \mathrm{Io}\ (4n+3) \times x_{Lm}\%} \tag{75}$$

4.3 | Number of primary, secondary, and tertiary winding turns of coupled inductor

The chosen value of the leakage inductor (L_k) is 3 μH. Thus, the value of magnetizing inductor by utilizing the coupling coefficient of the CI can be written as

$$L_m = \frac{3k \times 10^{-6}}{1-k} \tag{76}$$

Magnetic core E55/28/25 is chosen for the coupled inductor. Hence, depending on the dimensions that are considered in the core datasheet, the core air gaps of the CI can be expressed as

$$l_g = \frac{L_m {I_{Lm}}^2 \mu_0}{{B_m}^2 A_{Air\,\mathrm{Gap}}} = \frac{\frac{3k \times 10^{-6}}{1-k} \times \left(-\frac{\mathrm{Io}(4n+3)}{D-1}\right)^2 \times 4\pi \times 10^{-7}}{0.1^2 \times [(17.2+18.7) \times 25 \times 10^{-6}]} \tag{77}$$

By utilizing (77), the number of primary winding turns of the CI can be achieved by utilizing the following equation:

$$N_P \geq \sqrt{L_m \times \frac{l_g}{\mu_0 A_{Air\mathrm{Gap}}^{Equivalent}}} \tag{78}$$

The turns ratio of the CI is determined as $n_1 = N_S / N_P$ and $n_2 = N_t / N_P$. Thus, the number of secondary and tertiary winding turns of the coupled inductor can be expressed as

$$\begin{cases} N_S = n_1 \times N_P \Rightarrow N_S = 1.5 \times N_P \\ N_t = n_2 \times N_P \Rightarrow N_t = 1.5 \times N_P \end{cases} \tag{79}$$

5 | SMALL-SIGNAL MODELLING

All of the power semiconductors, the CI, and the capacitors are ideal. The CI has parasitic series resistors r_{Lm} and the parasitic series resistors of capacitors are r_C. Then, the average model and the small-signal model can be achieved via utilizing the state-space averaging method. The system equations in this method are obtained in all modes and they are averaged during single commutation time by taking into account the time interval of each mode. During all six switching subintervals, the system equations are written as

$$\begin{bmatrix} \dot{I}_{Lm} \\ \dot{V}_{C1} \\ \dot{V}_{C2} \\ \dot{V}_{C3} \\ \dot{V}_{C4} \\ \dot{V}_{C5} \\ \dot{V}_{CO} \end{bmatrix} = [A_m] \begin{bmatrix} I_{Lm} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \\ V_{CO} \end{bmatrix} + [B_m] V_{in} \tag{80}$$

where $m = 1, 2, 3, 4, 5, 6$.

The presented converter is controlled by utilizing the pole placement method and the small-signal model of the presented circuit is calculated and achieved from the state-space averaged model. Based on the small-signal modelling way, state variables, and control inputs which are comprised of two fixed ($\bar{X}$, $\bar{D}$) and variable ($\tilde{x}$, $\tilde{d}$) parts expressed as

$$\begin{cases} X = \bar{X} + \tilde{x} \\ D = \bar{D} + \tilde{d} \end{cases} \tag{81}$$

By utilizing it to the average model of the state space and via neglecting their square values, the small signal model of the suggested structure is obtained as

$$\begin{cases} \dot{\tilde{x}} = A\tilde{x} + B\tilde{u} \\ y = C\tilde{x} + D\tilde{u} \end{cases} \tag{82}$$

where variable states ($\tilde{x}$), control inputs ($\tilde{u}$), and output signals (y) are defined as follows:

$$\tilde{x}^T = \left[\tilde{i}_{Lm}\ \tilde{v}_{C1}\ \tilde{v}_{C2}\ \tilde{v}_{C3}\ \tilde{v}_{C4}\ \tilde{v}_{C5}\ \tilde{v}_{CO}\right] \tag{83}$$

$$\tilde{u} = \left[\tilde{d}\right] \tag{84}$$

$$y^T = \left[I_{Lm}\right] \tag{85}$$

Thus, A, B, D, and C matrices are expressed as follows:

$$\begin{bmatrix} \dot{\tilde{i}}_{Lm} \\ \dot{\tilde{v}}_{C1} \\ \dot{\tilde{v}}_{C2} \\ \dot{\tilde{v}}_{C3} \\ \dot{\tilde{v}}_{C4} \\ \dot{\tilde{v}}_{C5} \\ \dot{\tilde{v}}_{Co} \end{bmatrix} = 10^5 \times \overbrace{\begin{bmatrix} -0.0007 & -0.0035 & 0.0006 & -0.0012 & -0.0008 & 0.0012 & 0 \\ 0.0147 & -1.8401 & -0.4164 & -0.1369 & -0.6612 & 0.5536 & 0.4167 \\ -0.0041 & -0.7977 & -2.4333 & -0.3854 & 2.0022 & 0.3854 & 0 \\ 0.0051 & -0.3453 & -0.2710 & -1.5705 & -0.7707 & 0.5289 & 0.8333 \\ 0.0048 & 0.3451 & 2.0022 & -0.4480 & -3.0439 & -0.5937 & 0.8333 \\ -0.0051 & 0.3453 & 0.2710 & 0.3205 & -0.0626 & -1.7789 & 0.4167 \\ 0 & 0.6250 & 0 & 0.8333 & 1.0417 & 0.2083 & -0.8334 \end{bmatrix}}^{A} \times \begin{bmatrix} \tilde{i}_{Lm} \\ \tilde{v}_{C1} \\ \tilde{v}_{C2} \\ \tilde{v}_{C3} \\ \tilde{v}_{C4} \\ \tilde{v}_{C5} \\ \tilde{v}_{Co} \end{bmatrix} + \left(10^7 \times \overbrace{\begin{bmatrix} 0.0067 \\ -1.1130 \\ 0.0005 \\ -0.2785 \\ -0.2785 \\ 0.8339 \\ 0.2779 \end{bmatrix}}^{B} \tilde{d} \right) \tag{86}$$

$$I_{Lm} = \overbrace{\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}}^{C} \begin{bmatrix} \tilde{i}_{Lm} \\ \tilde{v}_{C1} \\ \tilde{v}_{C2} \\ \tilde{v}_{C3} \\ \tilde{v}_{C4} \\ \tilde{v}_{C5} \\ \tilde{v}_{CO} \end{bmatrix} + \overbrace{[0]}^{D} \tilde{d} \tag{87}$$

Based on the pole placement method, the poles of the closed loop could be located at any eligible position if the system is entirely state-controllable. The proposed converter's controllability matrix is written as

$$\Phi_C = \begin{bmatrix} B \vdots AB \vdots A^2B \vdots \cdots \vdots A^{n-1}B \end{bmatrix} \tag{88}$$

When the rank of the Φ_C is equal to 7 (rank of Φ_C equals the number of variable states ($\tilde{x}$)), the system is entirely controllable. Finally, two further integral states are determined as follows:

$$\dot{q}(t) = r(t) - y(t) = r(t) - \tilde{i}_{Lm}(t) \tag{89}$$

By utilizing the new integral states, both the state and output equations are rewritten as

$$\begin{bmatrix} \dot{\tilde{x}}(t) \\ \cdots \\ \dot{q}(t) \end{bmatrix} = \begin{bmatrix} A & \vdots & 0 \\ \cdots & \vdots & \cdots \\ -C & \vdots & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} + \begin{bmatrix} B \\ \cdots \\ 0 \end{bmatrix} \tilde{u}(t) + \begin{bmatrix} 0 \\ \cdots \\ I \end{bmatrix} r(t)$$
$$y(t) = \begin{bmatrix} C & \vdots & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} \tag{90}$$

In the above equation, $r(t)$ is the input reference vector which is expressed as follows:

$$r(t) = \begin{bmatrix} I_{Lm,ref} \end{bmatrix}^T \tag{91}$$

Based on (90), the new matrixes $\bar{A}$ and $\bar{B}$ are calculated as follows:

$$\bar{A} = \begin{bmatrix} A & \vdots & 0 \\ \cdots & \vdots & \cdots \\ -C & \vdots & 0 \end{bmatrix}, \bar{B} = \begin{bmatrix} B \\ \cdots \\ 0 \end{bmatrix} \tag{92}$$

The controllability matrix for the system in (90) could be defined as follows:

$$\bar{\Phi}_C = \begin{bmatrix} B & \vdots & A\Phi_C \\ \cdots & \vdots & \cdots \\ 0 & \vdots & -C\Phi_C \end{bmatrix} = \underbrace{\begin{bmatrix} B & \vdots & A \\ \cdots & \vdots & \cdots \\ 0 & \vdots & -C \end{bmatrix}}_{M} \begin{bmatrix} I & \vdots & 0 \\ \cdots & \vdots & \cdots \\ 0 & \vdots & \Phi_C \end{bmatrix} \tag{93}$$

If Φ_C is determined complete-rank, the system referred to in (90) is entirely controllable if the rank of the matrix M is $n + m$ (n and m are the number of the variable states ($\tilde{x}$) and output signals (y), respectively). Thus, there is a matrix K that is calculated as

$$\tilde{u}(t) = -K \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} = -\begin{bmatrix} K_x & \vdots & K_q \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} \tag{94}$$

where K_x and K_q are as follows:

$$\begin{aligned} K_x &= \begin{bmatrix} K_{11} & K_{12} & K_{13} & K_{14} & K_{15} & K_{16} & K_{17} \end{bmatrix} \\ K_q &= \begin{bmatrix} K'_{11} \end{bmatrix} \end{aligned} \tag{95}$$

Substituting (94) into (90) the following equation is

$$\begin{bmatrix} \dot{\tilde{x}}(t) \\ \cdots \\ \dot{q}(t) \end{bmatrix} = \begin{bmatrix} A - BK_x & \vdots & -BK_q \\ \cdots & \vdots & \cdots \\ -C & \vdots & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} + \begin{bmatrix} 0 \\ \cdots \\ I \end{bmatrix} r(t)$$

$$y(t) = \begin{bmatrix} C & \vdots & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} \tag{96}$$

To obtain proper values for Gain Margin and Phase Margin (GM≥10 and 60≤PM≤80), the trial and error method is utilized to consider the places of the closed-loop poles. By applying the process, the bode plot of the control system of the suggested converter is demonstrated in Figure 8. According to Figure 8, the values of the gain margin of inductor L_m are higher than 10 ($GM\,(i_{Lm}) > 10$) and the phase margin control (close-loop) path of i_{Lm} is 72.9726 which is appropriate. Figures 9 and 10 are the block diagram of the pole-placement control method and the current regulator loop of the coupled inductor, respectively.

6 | COMPARISON STUDY

To demonstrate the performance of the suggested converter, a comparison between the presented UHSU converter and other configurations is investigated. Table 1 demonstrates the features of the suggested converter and other configurations in terms of voltage gain, the normalized peak voltage of the power switch, maximum voltage stress on diodes, ZCS capability, number of components, and number of magnetic cores.

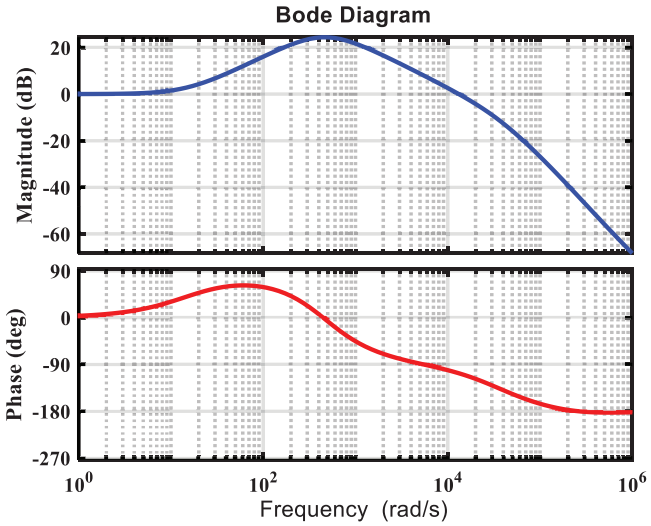

FIGURE 8 Bode diagram for the transfer function of the inductor current.

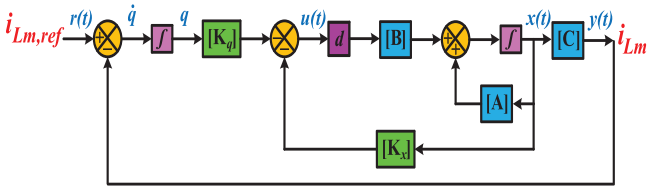

FIGURE 9 Block diagram of the pole-placement control method.

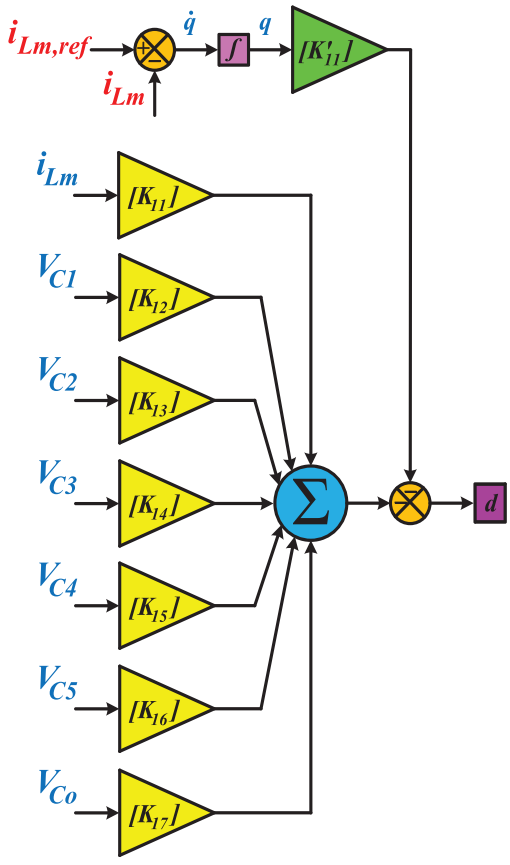

FIGURE 10 Current regulator loop of the coupled inductor.

TABLE 1 Comparison between the proposed converter and other structures.

Ref.	Voltage gain (for $n = 1.5$)	Normalized peak voltage (V_{switch}/V_o)	Maximum voltage stress on diodes	ZCS on the semiconductors	No. of components					No. of magnetic core/common ground
					S	D	C	L	CL	
Prop.	$\frac{(4n+3)}{1-D}$	$\frac{1}{4n+3}$	$\frac{(2n+1)V_O}{4n+3}$	Yes	1	6	6	0	1	1/No
[5]	$\frac{n(2-D)-D+4}{1-D}$	$\frac{1}{n(2-D)-D+4}$	$\frac{(n(2-D)-D)V_O}{n(2-D)-D+4}$	No	1	8	8	1	1	2/Yes
[22]	$\frac{3n+3}{1-D}$	$\frac{1}{3n+3}$	$\frac{(2n+1)V_O}{3n+3}$	No	1	5	6	1	1	2/Yes
[23]	$\frac{n(2-D)-D+1}{1-D}$	$\frac{1}{n(2-D)-D+1}$	$\frac{(n+1)V_O}{n(2-D)-D+1}$	Yes	1	4	5	1	1	2/Yes
[24]	$\frac{2(n+1)+n}{1-D}$	$\frac{1}{2(n+1)+n}$	$\frac{(3n+1)V_O}{2(n+1)+n}$	No	2	6	5	0	3	3/Yes
[25]	$\frac{3n+D+1}{1-D}$	$\frac{1}{3n+D+1}$	$\frac{(3n+1)V_O}{3n+D+1}$	Yes	2	6	7	2	3	5/Yes
[26]	$\frac{1+D+2n(1-D)}{(1-D)^2}$	$\frac{(1+D)}{1+D+2n(1-D)}$	$\frac{(2n)V_O}{1+D+2n(1-D)}$	No	2	4	4	1	1	2/Yes
[27]	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	$\frac{1}{3+2n-D(3+n-D)}$	$\frac{n(2-D)V_O}{3+2n-D(3+n-D)}$	No	2	5	5	1	1	2/Yes
[28]	$\frac{3n+2}{1-D}$	$\frac{1}{3n+2}$	$\frac{(2n+1)V_O}{3n+2}$	Yes	2	8	6	0	2	2/Yes
[29]	$\frac{4+2n}{1-D}$	$\frac{1}{4+2n}$	$\frac{(2n)V_O}{4+2n}$	Yes	2	6	6	0	2	2/No
[30]	$\frac{n(D-D^2)+nD+1}{(1-D)^2}$	$\frac{1}{n(D-D^2)+nD+1}$	$\frac{nV_O}{n(D-D^2)+nD+1}$	No	1	5	4	2	2	4/Yes
[31]	$\frac{1+n}{(1-D)^2}$	$\frac{1}{1+n}$	$\frac{nV_O}{1+n}$	Yes	1	5	4	1	1	2/Yes
[32]	$\frac{1+n-D}{(1-D)^2}$	$\frac{(1+n)(1-D)}{1+n-D}$	$\frac{nV_O}{1+n-D}$	No	1	5	3	1	1	2/Yes

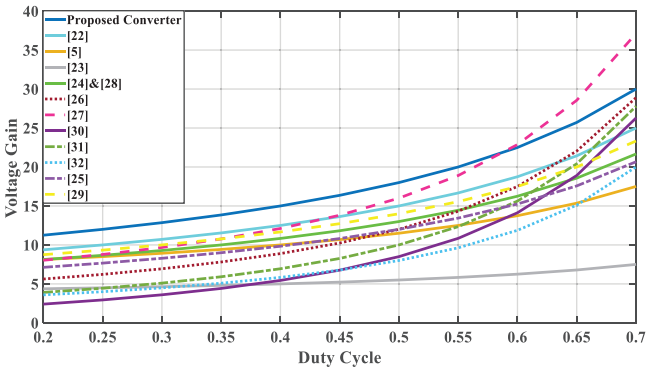

FIGURE 11 Voltage gain variations per different duty cycles for the compared step-up converters with $n = 1.5$.

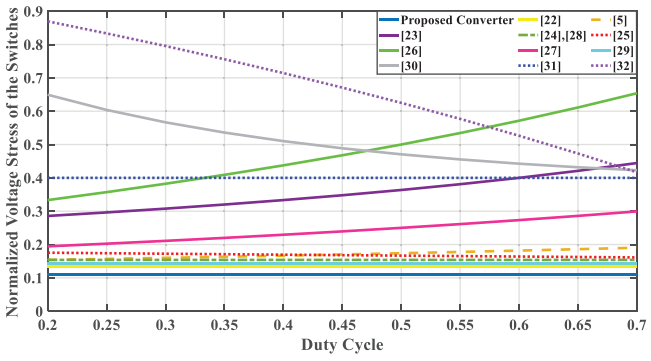

FIGURE 12 Comparison of the normalized voltage stress across the switches versus duty cycle ($n = 1.5$).

Table 1 consist of details of the converters in [5] and [22–32]. All the references that are utilized in Table 1 have CI structures. The topic of this paper is entitled UHSU converter and it considers voltage gain as the basic factor of the comparison. Figure 11 depicts voltage gain variations per different duty cycles for the compared step-up configurations that the shown curves are based on Table 1. According to the outcome, the voltage gain of the suggested converter is higher than the other structures. However, the UHSU structure in [27] boosts input voltage with a higher voltage gain per $D > 0.59$. The efficiency of the UHSU structure in [27] is a little more than 94% in 150 W power and $V_{in} = 20$ V, but the proposed configuration efficiency illustrated in Figure 6 is 96.28 in 150-W power and $V_{in} = 20$ V. Also, the number of utilized cores in [27] is two but the suggested structure has one core that diminishes the size and cost of the circuit. The proposed structure, compared with [27], has one power switch that makes a simple control process on the circuit, and the normalized voltage stress of the switches and diodes of the suggested circuit (as depicted in Figures 12 and 13) is lower than the structure in [27].

The third column of Table 1 display the normalized peak voltage of the power switches. The curve of the second column per different duty cycles is depicted in Figure 12. Figure 12 indicates that the normalized voltage stress of the switch in the suggested circuit is better than other configurations. Using a passive clamp circuit in the suggested configuration diminishes

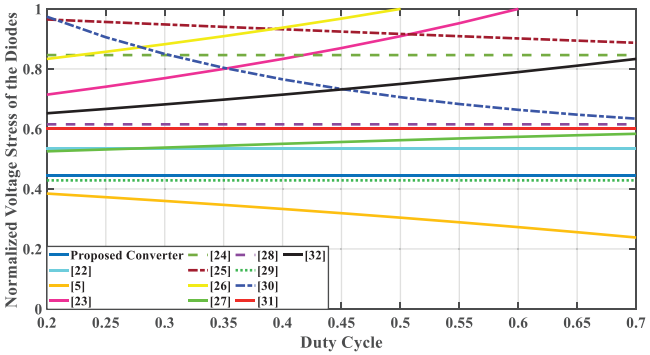

FIGURE 13 Comparison of the normalized voltage stress across the diodes versus duty cycle ($n = 1.5$).

the voltage across the power switch which leads to choosing a smaller inductor to the proposed circuit.

The fourth column of Table 1 illustrates the maximum voltage stress on diodes. The curve of the normalized voltage stress across the diodes per different duty cycles with $n = 1.5$ indicates the normalized voltage stress of the suggested configuration is lower than most of the other converters except [5] and [29]. The total number of components and inductor cores in [5] and [29] is higher than the suggested converter. The high number of components and inductor cores in [5] and [29] indicates the volume and the cost of the presented structure is less than them.

The fifth column of Table 1 shows the ZCS capability on semiconductor components. ZCS turn on and ZCS turn off exist in the proposed converter as depicted in Figure 4 that enhance the efficiency of the proposed converter. Unlike the proposed converter, the configurations in [5, 22, 24, 26, 27, 30], and [32] do not have ZCS capability on their semiconductor components.

The sixth column of Table 1 demonstrates the number of switches, diodes, capacitors, inductors, and CIs. The total number of the components in the suggested circuit is equal to or less than most of the UHSU and high step-up converters (equal to or less than structures in [5, 22, 24, 25, 27–29], and [30]), but the number of the components is not a good measurement. Table 2 displays a cost analysis comparing the proposed converter with other structures. Table 2 showcases that the cost of the suggested converter is the lowest. The approximated component costs were obtained from listings on AMAZON and EBAY websites and are succinctly presented in Table 2. Additionally, while the quantity of components may be substantial, the cost of these chosen components remains reasonable, largely attributed to their modest current and voltage ratings. Table 3 highlights the maximum peak current comparison between the showcased converter and other configurations.

The last column of Table 1 demonstrates the number of magnetic cores that include the sum of the number of inductors and the common ground capability of converters is illustrated in the last column. Number of the magnetic cores is significant and it must be less to suppress the size and cost of the configuration. Only the number of magnetic cores of the presented converter is one and the other structures have two or more than two magnetic cores.

ZCS, zero current switching.

The computation of the proposed converter's volume and size distribution is outlined in Table 4. Notably, the coupled inductor accounts for a substantial share of the overall volume. Following closely are the capacitors, with the high-voltage side capacitor being the dominant contributor to the volume. In comparison to other components, semiconductor devices make a relatively minor contribution. For purposes of comparison, the power density is also presented in Table 5. The proposed converter achieves a theoretical power density of 150 W per 68746.16 mm^3.

TABLE 2 Cost comparison between the proposed converter and other converters.

Ref	Cost of switches	Cost of diodes	Cost of capacitors	Cost of cores	Total cost
Prop	1 × 1.18 $	6 × 0.342 $	3 × 0.3145 $ 1 × 0799 $ 1 × 0.4495 $ 1 × 0.799 $	1 × 5.2 $	10.7039 $
[5]	1 × 2.754 $	8 × 0.774 $	6 × 2.99 $ 2 × 3.78 $	2 × 7.3932 $	49.23 $
[22]	1 × 1.18 $	5 × 0.342 $	5 × 0.599 $ 1 × 1.554 $	2 × 5.2 $	17.839 $
[23]	1 × 1.343 $	1 × 0.904 $ 3 × 0.712 $	2 × 0.266 $ 1 × 0.725 $ 1 × 0.4 $ 1 × 1.25 $	2 × 2.7325 $	12.755 $
[24]	2 × 2.43 $	6 × 0.342 $	4 × 0.95 $ 1 × 3.25 $	3 × 5.2 $	29.562 $
[25]	2 × 2.754 $	2 × 1.78 $ 2 × 2.3 $	6 × 0.95 $ 1 × 3.25 $	1 × 5.2 $ 4 × 2.7325 $	43.348 $
[26]	2 × 1.39 $	2 × 0.43 $ 2 × 0.995 $	2 × 2.59 $ 2 × 0.13 $	2 × 2.7325 $	16.535 $
[30]	1 × 2.883 $	1 × 0.36 $ 1 × 0.95 $ 2 × 0.413 $ 1 × 9.19 $	1 × 0.598 $ 3 × 1.089 $	4 × 3.604 $	32.49 $
[31]	1 × 0.925 $	2 × 0.88 $ 3 × 1.29 $	4 × 0.95 $	1 × 1.096 $ 1 × 3.25 $	14.701 $

TABLE 3 Maximum peak current comparison between the proposed converter and other converters.

Ref	Maximum peak current of switches	Maximum peak current of diodes
Pro[a]	$\frac{I_O(12n^2+10n+1)}{n(1-D)}$	$\frac{8I_O(n+2)}{1-D}$
[22]	$\left[\frac{4n_2+2n_3+D^2(n_2+1)-D(3n_2+n_3+2)+4}{D(1-D)}\right] I_o$	$\frac{I_O(2n_2+n_3+2)}{1-D}$
[23]	$\left(\frac{n\pi}{D}+M-n+1\right) I_O$	$I_O(M-n+1)$
[26]	$\frac{I_O}{1-D}+\frac{\pi n I_O}{2D}+MI_O$	$\frac{I_O(1+nD)}{(1-D)^2}$
[27]	$\left[\frac{[2+2n-D(2+n-D)]I_O}{D(1-D)^2}+\frac{DV_{in}}{2L_1 f_s}\right]$	$\left[\frac{[2+2n-D(2+n-D)]I_O}{(1-D)^2}+\frac{DV_{in}}{2L_1 f_s}\right]$

[a]**Pro**: Proposed Converter.

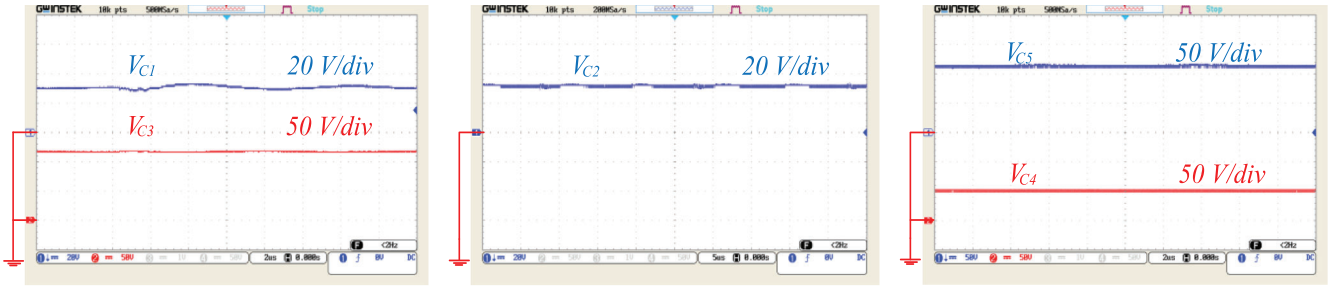

FIGURE 14 The experimental voltage waveforms of capacitors: (a) voltage across the capacitors C_1 and C_3, (b) voltage across the capacitor C_2, (c) voltage across the capacitors C_4 and C_5.

TABLE 4 Power density of the proposed converter.

Components	Specification	Volume
Switches	IRFP260n Length: 36.10 mm Width: 15.87 mm Thickness: 5.21 mm	2984.84 mm^3
Diodes	Mur1560G Length: 15.88 mm Width: 10.29 mm Thickness: 4.83 mm	$6 \times 789.24 = 4735.44$ mm^3
Capacitors	C_1,C_4,C_5 Diameter: 6.3 mm Height: 11 mm C_2 Diameter: 5 Height: 11 C_3 Diameter: 13 Height: 20 C_O Diameter: 16 Height: 25	$(3\times342.90) + (215.98) + (2654.65) + (5026.55) = 8925.88$ mm^3
Coupled inductor	EE55/28/25 core	52,100 mm^3
	Total volume:	68,746.16 mm^3
	Power density:	2.181 mW/mm^3

The comparisons accredit the higher voltage gain of the suggested configuration and the lower voltage stress on its power switches and diodes. Plus, because of the low voltage stress of the power switch, the presented circuit requires a small inductor.

7 | EXPERIMENTAL RESULTS

In the proposed converter, to verify the theoretical analysis and accurate performance of the suggested converter a 150-W experimental prototype is manufactured. The main characteristic of the suggested step-up converter is given in Table 6. According to Figure 14a, the voltages across the capacitors C_1 and C_3 are 30 and 120 V, respectively. Also, the voltage across the capacitor C_2 is 32 V as shown in Figure 14b. The voltages across the capacitors C_4 and C_5 are 50 and 110 V, respectively, as illustrated in Figure 14c. The voltage across the utilized single power switch is measured 29 V and was demonstrated in Figure 15a along with the current of the power switch that is measured 20 A. Figure 15b illustrates the voltage and current of output that are measured as 290 V and 0.4 A, respectively. The voltage of the input source is indicated in Figure 15c along with the current of the input source which is 20 V and 22 A, respectively. Figure 16a shows the measured voltage and current of the diode D_1 which are 27 V and 26 A, respectively. Also, the voltage across the diode D_2 along with the current of diode D_2 is demonstrated in Figure 16b and measured 78 V and 4 A, respectively. As well as Figure 16b demonstrated ZCS on diode D_2. Figure 16c depicts the voltage and current of the diode D_3 and the values are 44 V and 2 A, respectively. In Figure 16d the voltage of diode, D_4 is 130 V and its current is equal to 2 A. Voltage and currents of diode D_5 are 132 V and 2 A, respectively, as displayed in Figure 16e. Figure 16f presents the voltage and current of diode D_o. The voltage of diode D_O is measured 130 V and the current of D_o is measured 4 A and ZCS on diode D_O is illustrated in Figure 16f. Figures 14–16 illustrate the experimental results of the proposed converter are close to the obtained equations.

8 | CONCLUSIONS

In this paper, a non-isolated single-switch UHSU DC–DC converter with a coupled inductor base is presented. The voltage gain of the proposed UHSU converter is increased via raising the turn ratio of the CI. In addition, the normalized voltage stress across the power switch is decreased by the passive clamp circuit. The main merits of the suggested configuration comprised of high-voltage gain with high efficiency, ZCS of power diodes in ON-state and OFF-state, low voltage stress across the semiconductors, two degrees of freedom to control the converter's voltage gain (duty cycle and the turns-ratio of the CIs), simple control process because of using one power switch, achieving high-voltage gains without duty cycle limitation and generating high output voltage with a small duty cycle that reduces the conduction loss of the single switch.

TABLE 5 Power density comparison between the proposed converter and other converters.

Ref	S.V* (mm3)	D.V* (mm3)	C.V* (mm3)	I.V* (mm3)	T.V* (mm3)	P.D* (mm3)
Pro	2984.84	4735.44	8925.88	52100	68746.16	150 W/68746.16 = 2.181 mW/mm3
[5]	3101.12	11910.88	6193.80	99400	120605.8	200 W/120605.8 = 1.658 mW/mm^3
[22]	2984.84	3946.2	45529.53	104200	156660.57	240 W/156660.57 = 1.531 mW/mm^3
[23]	1605.14	1713.82	16987.38	34600	54906.34	100 W/54906.34 = 1.821 mW/mm^3
[24]	9623.06	4735.44	56253.36	156300	226911.86	1300 W/226911.86 = 5.729 mW/mm^3
[25]	6202.24	8541.56	66708.58	109700	191152.38	1000 W/191152.38 = 5.231 mW/mm^3
[26]	3210.28	3719.974	16474.52	34600	58004.774	1000 W/58004.774 = 3.447 mW/mm^3
[30]	3593.506	5138.29	18585.65	408000	435317.44	1000 W/435317.44 = 2.297 mW/mm^3
[31]	54.25	4176.618	20910.44	5040	30181.308	50 W/30181.308 = 1.656 mW/mm^3

*__C.V__, capacitors volume; *__D.V__, diodes volume; *__I.V__, inductors volume; *__P.D__, power density; *__S.V__, switches volume; *__T.V__, total volume.

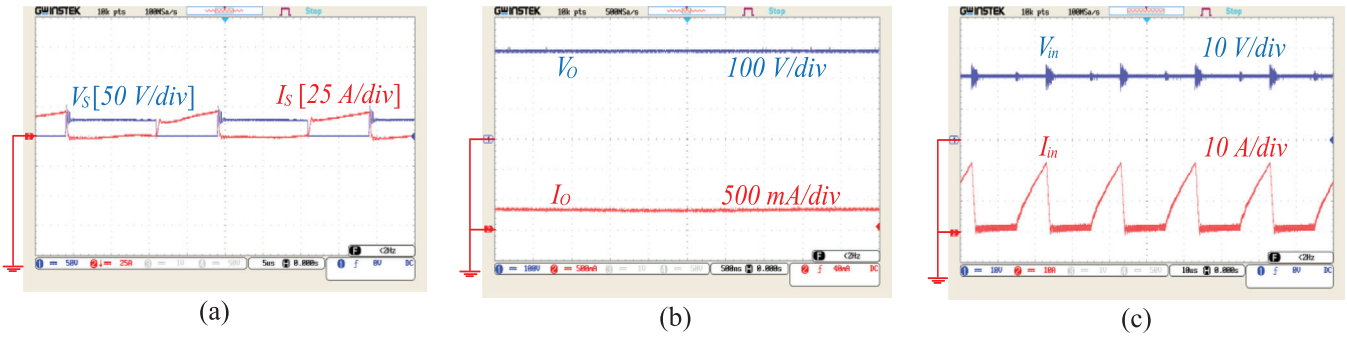

FIGURE 15 The experimental waveforms of power switch, output port and input source, (a) voltage and current of the power switch, (b) voltage and current of the output port, (c) voltage and current of the input source.

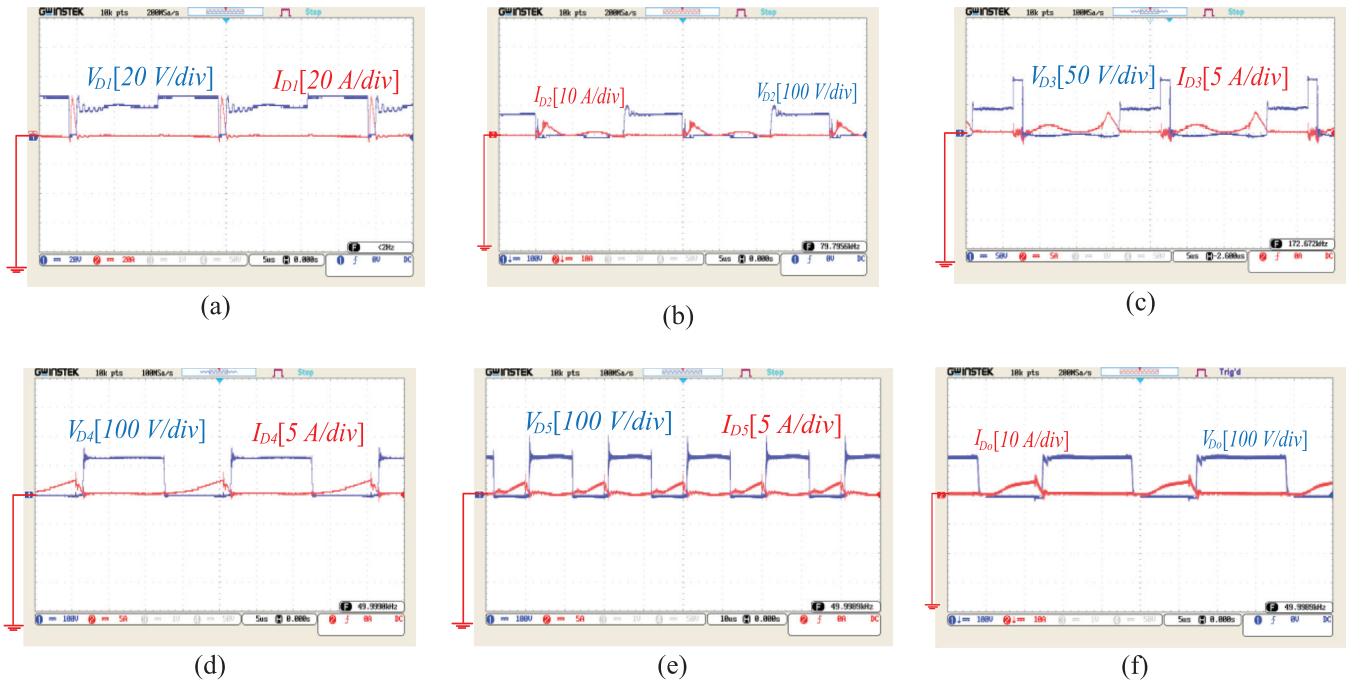

FIGURE 16 The experimental waveforms of diodes, (a) voltage and current of the diode D_1, (b) voltage and current of the diode D_2, (c) voltage and current of the diode D_3, (d) voltage and current of the diode D_4, (e) voltage and current of the diode D_5, (f) voltage and current of the diode D_O.

TABLE 6 Component characteristic of the implemented converter.

Rated power (P_o)	150 W
Input voltage	20 V
Output voltage	300 V
Switching frequency (f_s)	50 kHz
Turns ratio n_1 (N_S/N_P), n_2 (N_t/N_P)	1.5, 1.5
Magnetizing inductor (L_m)	500 μH
Leakage inductor (L_k)	3 μH
Power switch	IRFP260n
Diodes	Mur1560 G
Capacitor (C_2)	10 μF/63 V
Capacitors (C_1, C_4,C_5,)	22 μF/100 V
Capacitor (C_3)	22 μF/250 V
Capacitor (C_o)	47 μF/450 V

AUTHOR CONTRIBUTIONS

Ali Nadermohammadi: Formal analysis; methodology; software; writing—original draft. **Mohammad Maalandish**: Formal analysis; methodology; project administration; validation; writing—review & editing. **Ali Seifi**: Formal analysis; software; validation; writing—review & editing. **Seyed Hossein Hosseini**: Project administration; supervision; validation; writing—review & editing. **Murtaza Farsadi**: Formal analysis; validation; writing—review & editing.

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The authors have nothing to report.

CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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